

PTO/SB/08A (10-01)

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Substitute for form 1449A/PTO		<b>Complete if Known</b>			
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application Number	09/243,825		
		Filing Date	June 25, 1999		
		First Named Inventor	Derek Wong		
		Art Unit	2183		
		Examiner Name	Eric Coleman		
Sheet	1	of	2	Attorney Docket Number	

U.S. PATENT DOCUMENTS					
Examiner Initials <sup>2</sup>	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
E.C.	1	US- 5,630,082	05-13-1997	N. Yao et al	
	2	US- 5,651,125	07-22-1997	D. Witt et al	
	3	US- 5,481,743	01-02-1996	M. Baxter	
	4	US- 5,446,912	08-29-1995	R. Colwell et al	
	5	US- 5,632,023	05-20-1997	S. White et al	
E.C.		US-			
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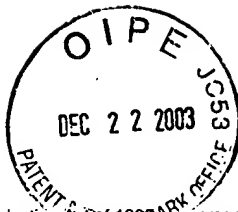
FOREIGN PATENT DOCUMENTS						
Examiner Initials <sup>2</sup>	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

Examiner Signature		Date Considered	3/19/04
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		Group Art Unit	2183		
		Examiner Name	Eric Coleman		
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
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C.C.	6	J. JOHNSON, <u>Expansion Caches for Superscalar Machines</u> , A Doctoral Dissertation in Electrical Engineering Department at Stanford University, March 1996, 183 pages, Stanford, CA, USA. File downloaded from Internet.	
	7	E. ROTENBERG ET AL, "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings of the 29 <sup>th</sup> Annual Symposium on Microarchitecture, December 2-4, 1996, IEEE, New Jersey, USA. File downloaded from Internet.	
	8	E. ROTENBERG ET AL, "Trace Processors", Proceedings of Micro-30, December 1-3, 1997, IEEE, New Jersey, USA. File downloaded from Internet.	
	9	J. CRAWFORD AND J. HUCK, "Next Generation Instruction Set Architecture". Presentation slides from 1997 Microprocessor Forum conference. October 14, 1997, San Jose, CA. File downloaded from intel.com Web site.	
	10	J. CRAWFORD AND J. HUCK, "Motivations and Design Approach for the IA-64 64-bit Instruction Set Architecture." Transcript from 1997 Microprocessor Forum conference. October 14, 1997, San Jose, CA. File downloaded from intel.com Web site.	
	11	INTEL, "The Next Generation of Microprocessor Architecture: A 64-bit Instruction Set Architecture (ISA) based on EPIC Technology" -- a Web page. October 1997. Web page downloaded from intel.com Web site.	
	12	D. GALLAGHER ET AL, "Dynamic Memory Disambiguation Using the Memory Conflict Buffer", Proceedings of ASPLOS-VI conference, October 1994. File downloaded from Internet.	
	13	K. WANG and M. FRANKLIN, "Highly Accurate Data Value Prediction using Hybrid Predictors", Proceedings of Micro 30. December 1-3, 1997, IEEE, New Jersey, USA. File downloaded from Internet.	
	14	D. AUGUST ET AL, "A Framework for Balancing Control Flow and Predication", 1997 paper, Center for Reliable and High Performance Computing, University of Illinois, Urban-Champaign, IL. File downloaded from Internet.	
	4.C.	15	S. MAHLKE ET AL, "A Comparison of Full and Partial Predicated Execution Support for ILP Processors", ISCA-22, June 1995. Center for Reliable and High Performance Computing, University of Illinois, Urban-Champaign, IL. File downloaded from Internet.

Examiner Signature	<i>Eric Coleman</i>	Date Considered	3/19/04
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